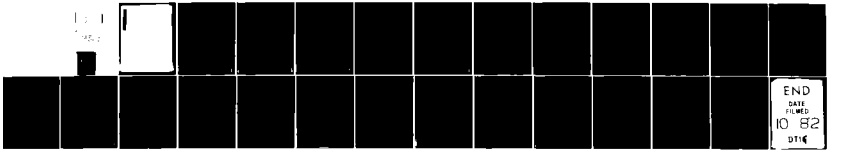
AD-A119 323 NAVAL RESEARCH LAB WASHINGTON DC F/G 9/2
CAMAC: A UNIQUE APPLICATION WITH A POCKET TERMINAL.(U)
SEP 82 A D ELMOND
UNCLASSIFIED NRL-MR-4897 NL



SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

| REPORT DOCUMENTATION PAGE | | READ INSTRUCTIONS BEFORE COMPLETING FORM |
|---|---|---|
| 1. REPORT NUMBER<br>NRL Memorandum Report 4897 | 2. GOVT ACCESSION NO.<br>AD-A119323 | 3. RECIPIENT'S CATALOG NUMBER |
| 4. TITLE (and Subtitle)<br>CAMAC: A UNIQUE APPLICATION WITH A POCKET TERMINAL | | 5. TYPE OF REPORT & PERIOD COVERED<br>Final report<br>6. PERFORMING ORG. REPORT NUMBER |
| 7. AUTHOR(s)<br>A.D. Elmond | | 8. CONTRACT OR GRANT NUMBER(s) |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS<br>Naval Research Laboratory<br>Washington, D.C. 20375 | | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS<br>77-G322-A2 |
| 11. CONTROLLING OFFICE NAME AND ADDRESS | | 12. REPORT DATE<br>September 16, 1982<br>13. NUMBER OF PAGES<br>24 |
| 14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) | | 15. SECURITY CLASS. (of this report)<br>UNCLASSIFIED<br>15a. DECLASSIFICATION/DOWNGRADING SCHEDULE |

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES



19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

| | | |
|---|---|---|
| CAMAC | IEEE Standard 583 | Processing |
| Commands | Hardware | Routine |
| Computer system | I/O handler | Terminal |
| Data collection | Microprocessor | |

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

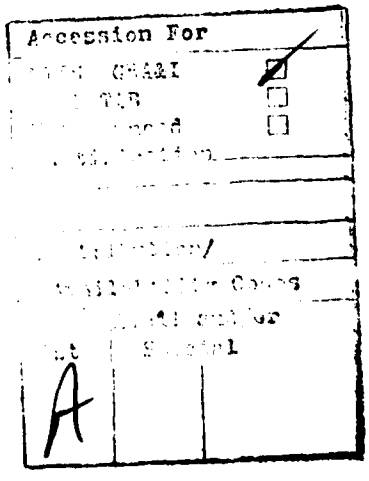
Computer Automated Measurement and Control (CAMAC), IEEE's Standard 583, is being employed to upgrade a computer controlled, data collection and processing system in the Navy Space Program. This report describes an implementation of this standard for this project. A portable pocket terminal is used to perform standard operations of the CAMAC specifications.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

## CONTENTS



# CAMAC: A UNIQUE APPLICATION WITH A POCKET TERMINAL

## I Introduction

Requirements to improve the capability of a computer controlled, data collection and processing system for a Navy Space Project demanded an innovative design. This design included the use of microprocessors and the adoption of a data bus standard to allow functional units to communicate with each other, with peripherals, and with the computer.

Computer Automated Measurement and Control (CAMAC), IEEE's Standard 583, is a bus standard for microprocessors. Because it is an accepted standard for data acquisition and control applications, CAMAC was chosen to upgrade this computer controlled, data collection and processing system. The system is composed of unique state-of-the-art electronic equipments. The use of CAMAC offered significant advancement in increasing the system's flexibility, reducing special purpose hardware and software, and extending the system's useful life. These are requirements for this data collection system. CAMAC equipment, acquired from many sources, has been integrated into efficient, reliable control systems demonstrating the advantages of standardized module design and of the interchangeability of functions on a hardware module basis.

CAMAC also provided an alternate approach to central processing, distributed processing, which places a far smaller processing burden on the host computer. Distributed processing offered an improvement in system performance by providing the capability to process data in parallel. This feature is important to accommodate any new requirements which may be levied in the future.

*Manuscript submitted July 20, 1982.*

## II CAMAC Description

The CAMAC standard goes well beyond a simple hardware intercommunication convention and specifies a parallel interface bus together, with specific physical modules, the crates. The CAMAC module is the basic unit of the CAMAC system and interfaces the CAMAC system and real-world external processes. An 86-pin connector terminates each module.

The CAMAC crate houses, powers, cools, and provides dataway communications for the CAMAC modules and crate controller. A crate controller resides at the end of every crate.

The dataway provides separate dedicated lines for station addresses (N) and interrupts (L). The N lines allow the controller to address modules individually or in combination. The L lines allow the modules to request servicing by the controller. The IEEE CAMAC Standard specifies the physical dimensions, power requirements, signal levels and module responses to commands. A CAMAC system is illustrated by figure 1.

## III CAMAC Operations

The LSI-11 CAMAC Crate Controller uses an addressing method called "memory mapping" to provide an interface between Digital Equipment Corporation's LSI 11 computer bus and the IEEE 583 bus. An operation on the IEEE 583 bus is defined by 3 parameters: (1) Ø-23 Station Numbers (N), (2) Ø-15 Subaddresses (A), and (3) Ø-31 Function Codes (F). Every possible combination of (N) and (A) is represented by a register in the computer I/O area. This is a total of 23 * 16 = 368 registers. In any operation, N and A is determined by which of these registers is used to perform the operation. The general method for transferring data is to store to or read from one of these registers.

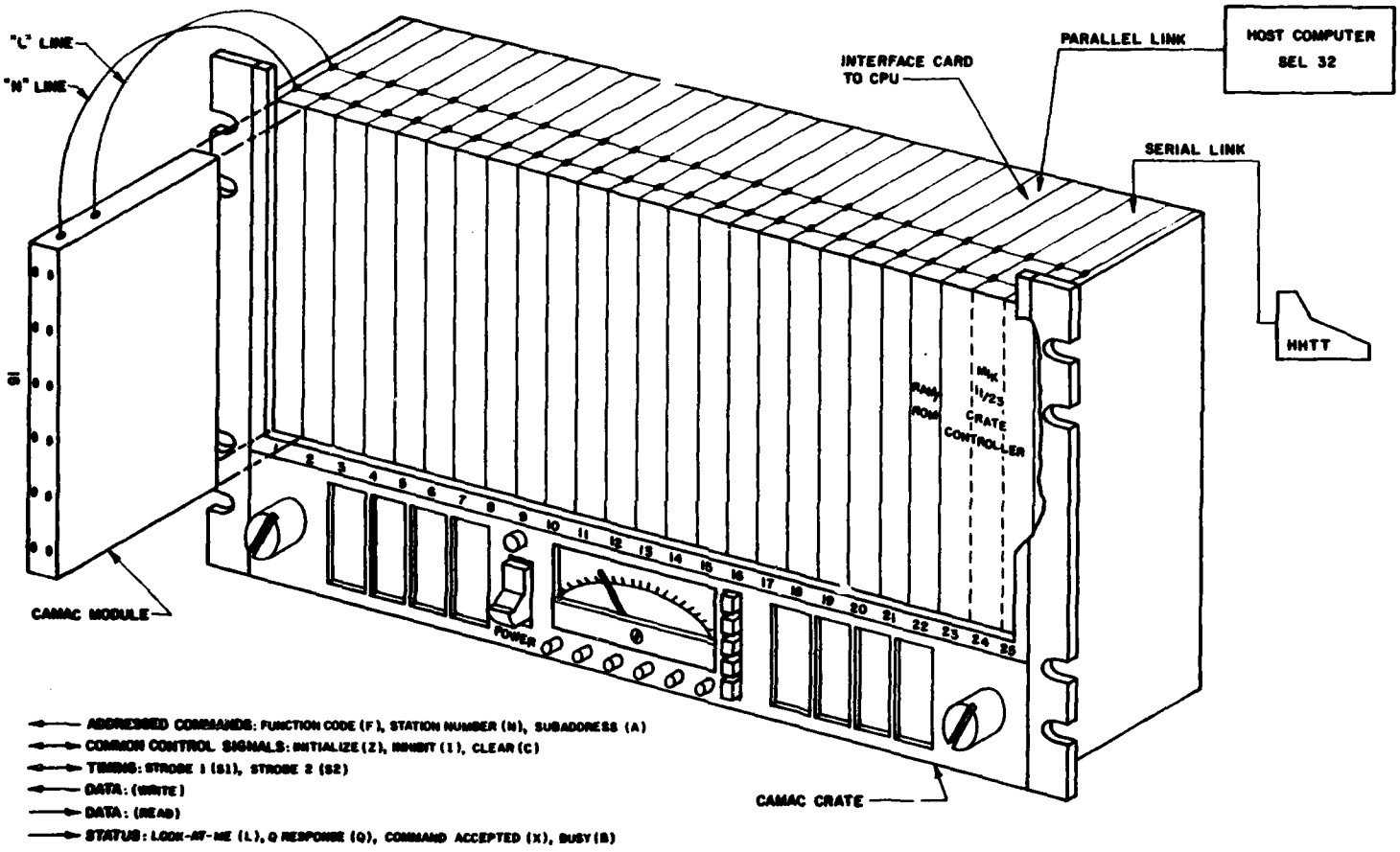



**Fig. 1 — IEEE 583, CAMAC interface standard**

The function to be performed at the subaddress (A) in the selected module (N) is defined by IEEE Standard 583 and the operation of the controller. The definitions of the thirty-two function codes are summarized in figure 2. Two major operations are defined by these function codes: Control/test operations and data transfer operations. Data transfer operations are defined by F8=Ø. The direction of the transfer is defined by F16, F16=Ø indicates a read and F16=1 indicates a write. Control/test operations are defined by F8=1 and no data is associated with it. I/O operations are performed by an I/O handler.

## IV The CAMAC I/O Handler

The basic elements of the operation of the I/O handler are found in the Input Output Transfer Block (IOTB) and the Input Output Transfer List (IOTL). These two data areas allow the I/O Handler to perform many different types of transfers under the control of the user.

The main objective of the I/O Handler is to provide the capability for many types of transfers. In the CAMAC Crate there can be many different types of modules requiring various communication modes on the dataway. Examples of these modes are 16 bit transfers versus 24 bit transfers, or buffered data transfer versus non-buffered. The I/O Handler concept allows the transfer initiation to set up the type of transfer and have the I/O Handler perform it.

One of the requirements levied during the initial design phase was that all dataway communication between modules would be through the CAMAC Controller. That concept is made possible through the use of the I/O Handler. Each call to the I/O Handler is accompanied by the address of a Control/Status Word (CSW) followed by a 5 word table called

| CODE F( ) | FUNCTION | USE OF R AND W LINES | FUNCTION SIGNALS | | | | | CODE F( ) |
|---|---|---|---|---|---|---|---|---|
| | | | F16 | F8 | F4 | F2 | F1 | |
| 0 | Read Group 1 Register | Functions using the R lines | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | Read Group 2 Register | | 0 | 0 | 0 | 0 | 1 | 1 |
| 2 | Read and Clear Group 1 Register | | 0 | 0 | 0 | 1 | 0 | 2 |
| 3 | Read Complement of Group 1 Register | | 0 | 0 | 0 | 1 | 1 | 3 |
| 4 | Non-standard | | 0 | 0 | 1 | 0 | 0 | 4 |
| 5 | Reserved | | 0 | 0 | 1 | 0 | 1 | 5 |
| 6 | Non-standard | | 0 | 0 | 1 | 1 | 0 | 6 |
| 7 | Reserved | | 0 | 0 | 1 | 1 | 1 | 7 |
| 8 | Test Look-at-Me | Functions not using the R or W lines | 0 | 1 | 0 | 0 | 0 | 8 |
| 9 | Clear Group 1 Register | | 0 | 1 | 0 | 0 | 1 | 9 |
| 10 | Clear Look-at-Me | | 0 | 1 | 0 | 1 | 0 | 10 |
| 11 | Clear Group 2 Register | | 0 | 1 | 0 | 1 | 1 | 11 |
| 12 | Non-standard | | 0 | 1 | 1 | 0 | 0 | 12 |
| 13 | Reserved | | 0 | 1 | 1 | 0 | 1 | 13 |
| 14 | Non-standard | | 0 | 1 | 1 | 1 | 0 | 14 |
| 15 | Reserved | | 0 | 1 | 1 | 1 | 1 | 15 |
| 16 | Overwrite Group 1 Register | Functions using the W lines | 1 | 0 | 0 | 0 | 0 | 16 |
| 17 | Overwrite Group 2 Register | | 1 | 0 | 0 | 0 | 1 | 17 |
| 18 | Selective Set Group 1 Register | | 1 | 0 | 0 | 1 | 0 | 18 |
| 19 | Selective Set Group 2 Register | | 1 | 0 | 0 | 1 | 1 | 19 |
| 20 | Non-standard | | 1 | 0 | 1 | 0 | 0 | 20 |
| 21 | Selective Clear Group 1 Register | | 1 | 0 | 1 | 0 | 1 | 21 |
| 22 | Non-standard | | 1 | 0 | 1 | 1 | 0 | 22 |
| 23 | Selective Clear Group 2 Register | | 1 | 0 | 1 | 1 | 1 | 23 |
| 24 | Disable | Functions not using the R or W lines | 1 | 1 | 0 | 0 | 0 | 24 |
| 25 | Execute | | 1 | 1 | 0 | 0 | 1 | 25 |
| 26 | Enable | | 1 | 1 | 0 | 1 | 0 | 26 |
| 27 | Test Status | | 1 | 1 | 0 | 1 | 1 | 27 |
| 28 | Non-standard | | 1 | 1 | 1 | 0 | 0 | 28 |
| 29 | Reserved | | 1 | 1 | 1 | 0 | 1 | 29 |
| 30 | Non-standard | | 1 | 1 | 1 | 1 | 0 | 30 |
| 31 | Reserved | | 1 | 1 | 1 | 1 | 1 | 31 |

Fig. 2 — Standard CAMAC function codes

Input-Output Transfer Block (IOTB) (See figure 3). A series of IOTB tables, called an Input-Output Transfer List (IOTL), may be loaded as long as they are in contiguous memory locations following the status word. Upon completion or abortion of an operation, the corresponding IOTB will contain certain information about the operation. The format of an IOTB status word is shown below.

The Dataway User is responsible for words 0, 1, 2, and 4 of the IOTB. The I/O Handler will return information in the Control Status Word (CSW) and Word 3. Bits 0, 1, and 2 of Word Ø contain Handler commands and will be supplied by the user.

The Control/Status word allows the user to maintain the progress of data transfers by keeping a running tally on IOTB's that complete execution.

| | |
|---|---|
| Bit Ø | EB - The Error Bit (EB) is set by the I/O Handler when an error occurs during a Dataway Transfer. |
| Bits 1-7 | Unused |
| Bits 8-15 | IOTB Count - Contains the count of the last IOTB executed correctly. |

## CONTROL / STATUS WORD (CSW)

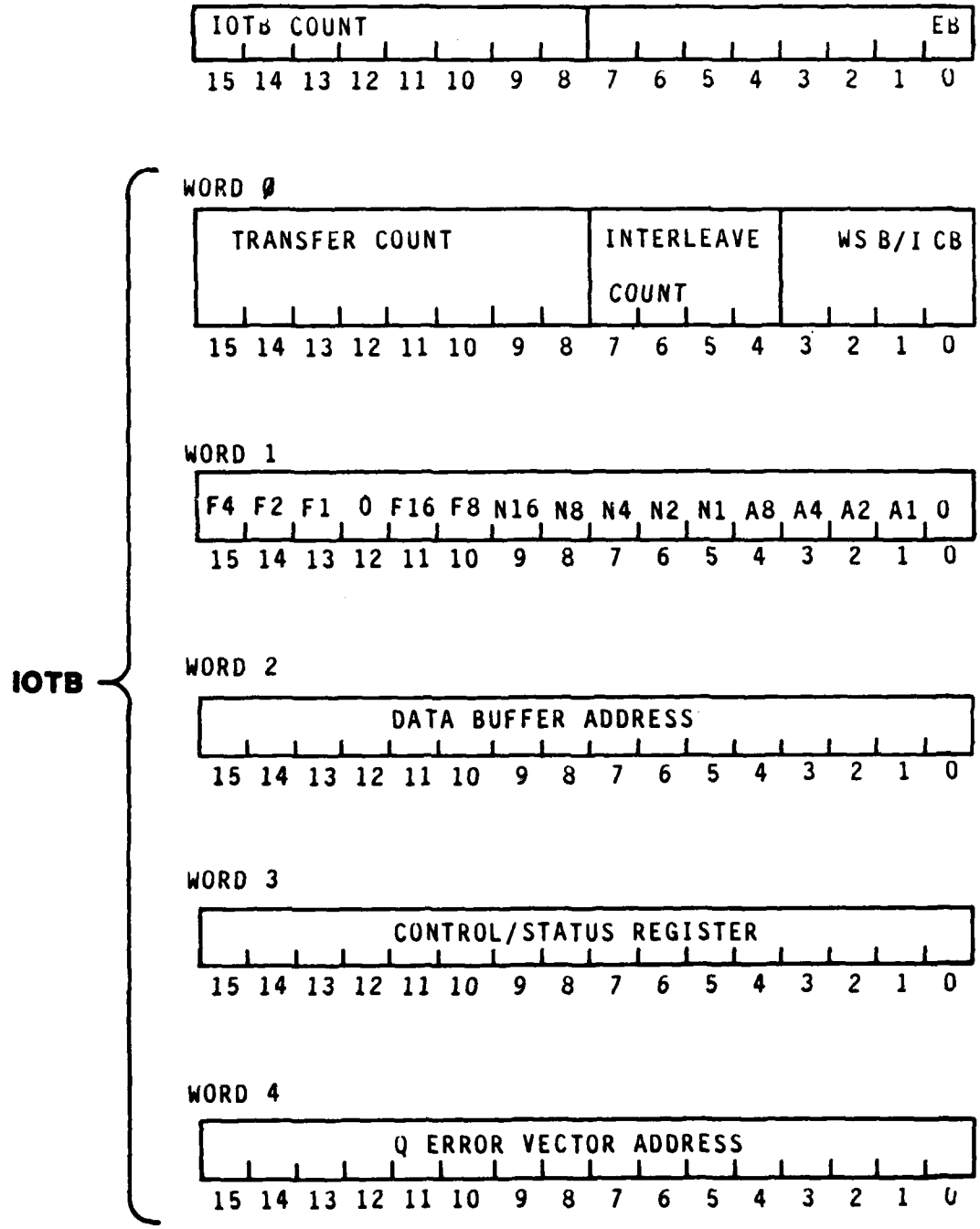



Fig. 3 — Control/status word IOTB format

## Input/Ouput Transfer Block

The IOTB is the heart of the Handler it stores all the necessary information for the Handler to make transfers. A description of all 5 words is given below.

### Word Ø

| | |
|---|---|
| Bit Ø | CB - The Control Bit (CB) is set by the CAMAC Dataway User to indicate IOTL tracking. The last IOTB will have this bit set to indicate the last IOTB in the IOTL. |
| Bit 1 | B/I - This bit is used to indicate the buffered or Interleaved Mode. Bit not set indicates Buffered Mode and bit set indicates Interleave Mode. |
| Bit 2 | WS - The word size (WS) bit is set by the CAMAC Dataway user to indicate a 16 or 24 bit data word transfer. Bit set = 24 bit data word transfer, and bit not set = 16 bit data word transfer. |
| Bit 3 | Unused |
| Bits 4 - 7 | Interleave Count - An interleave count is passed to the I/O Handler if the Interleave mode is indicated by bit 1 and indicates the number of transfers requested by the CAMAC Dataway User. |

Bits 8 - 15 — Transfer Count - This field is supplied by the Dataway User to indicate the number of Dataway transfers requested for a given IOTB and will contain the residual transfer count when an error occurs. It should be zero on normal termination. The maximum number of transfers is 256.

Word 1

Bits 0 - 15 — NAF - These bits are defined in figure 4 and are supplied by the Dataway user.

Word 2

Bits 0 - 15 — Data Buffer Address - This 16 bit field is supplied by the Dataway user and contains the address of the beginning of the data buffer to be used in data transfer. The next sequential location or residual address will be returned on error at end of transfer.

Word 3

Bits 0 - 15 — Control/Status Register - Word 3 is returned by the I/O Handler when an error occurs on a Dataway transfer. An error is indicated by bit Ø of the CSW. See figure 5.

Word 4

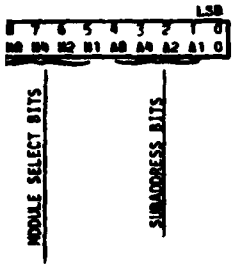
Bits 0 - 15 — Q Error Vector Address - The I/O Handler checks the Q line after every transfer. A Q=1 indicates a good transfer and a Q=0 indicates that the transfer was not accepted. The transfer is retried a specified number of times and if a valid transfer does not occur, the I/O Handler returns to the calling routines Q Error Vector Address.

Each IOTB is used by the handler to perform a transfer between the controller and a module. The IOTB sets, (whether the transfer is a single or multiple word) word size 24 bit or 16 bit and mode of operation Buffered or Interleave.

Interleave Mode

Single data transfers require that a NAF (see figure 4) be sent for each transfer. A method is needed for the user to send/receive multiple single data transfers after a link is established with a target module. The interleave mode provides this capability. It allows the user to establish this link, send a transfer count, and then send/receive the required number of single data transfers.

When in the Interleaved Mode, the user must build an IOTL consisting of two IOTBs to pass to the I/O Handler. The first IOTB is built for reading from a module and the second IOTB is built for writing to another module. This effect creates module to module data transfers.




**OPTION TABLE**

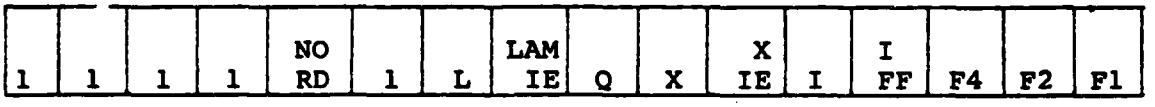
| Code F() | Function | Use of R and W Lines | F16 | Function Signals F8 | F4 | F2 | F1 | Code F() |
|---|---|---|---|---|---|---|---|---|
| 0 | Read Group 1 register | Functions using the R lines | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | Read Group 2 register | | 0 | 0 | 0 | 0 | 1 | 1 |
| 2 | Read and Clear Group 1 register | | 0 | 0 | 0 | 1 | 0 | 2 |
| 3 | Read Complement of Group 1 register | | 0 | 0 | 0 | 1 | 1 | 3 |
| 4 | Nonstandard | | 0 | 0 | 1 | 0 | 0 | 4 |
| 5 | Reserved | | 0 | 0 | 1 | 0 | 1 | 5 |
| 6 | Nonstandard | | 0 | 0 | 1 | 1 | 0 | 6 |
| 7 | Reserved | | 0 | 0 | 1 | 1 | 1 | 7 |
| 8 | Test Look-at-Me | Function not using the R or W | 0 | 1 | 0 | 0 | 0 | 8 |
| 9 | Clear Group 1 register | | 0 | 1 | 0 | 0 | 1 | 9 |
| 10 | Clear Look-at-Me | | 0 | 1 | 0 | 1 | 0 | 10 |
| 11 | Clear Group 2 register | | 0 | 1 | 0 | 1 | 1 | 11 |
| 12 | Nonstandard | | 0 | 1 | 1 | 0 | 0 | 12 |
| 13 | Reserved | | 0 | 1 | 1 | 0 | 1 | 13 |
| 14 | Nonstandard | | 0 | 1 | 1 | 1 | 0 | 14 |
| 15 | Reserved | | 0 | 1 | 1 | 1 | 1 | 15 |
| 16 | Overwrite Group 1 register | Functions using the W lines | 1 | 0 | 0 | 0 | 0 | 16 |
| 17 | Overwrite Group 2 register | | 1 | 0 | 0 | 0 | 1 | 17 |
| 18 | Selective Set Group 1 register | | 1 | 0 | 0 | 1 | 0 | 18 |
| 19 | Selective Set Group 2 register | | 1 | 0 | 0 | 1 | 1 | 19 |
| 20 | Nonstandard | | 1 | 0 | 1 | 0 | 0 | 20 |
| 21 | Selective Clear Group 1 register | | 1 | 0 | 1 | 0 | 1 | 21 |
| 22 | Nonstandard | | 1 | 0 | 1 | 1 | 0 | 22 |
| 23 | Selective Clear Group 2 register | | 1 | 0 | 1 | 1 | 1 | 23 |
| 24 | Disable | Functions not using the R or W lines | 1 | 1 | 0 | 0 | 0 | 24 |
| 25 | Execute | | 1 | 1 | 0 | 0 | 1 | 25 |
| 26 | Enable | | 1 | 1 | 0 | 1 | 0 | 26 |
| 27 | Test Status | | 1 | 1 | 0 | 1 | 1 | 27 |
| 28 | Nonstandard | | 1 | 1 | 1 | 0 | 0 | 28 |
| 29 | Reserved | | 1 | 1 | 1 | 0 | 1 | 29 |
| 30 | Nonstandard | | 1 | 1 | 1 | 1 | 0 | 30 |
| 31 | Reserved | | 1 | 1 | 1 | 1 | 1 | 31 |

(1) - See option table for functions codes

(2) - 1 = data write from controller to selected module (most data transfer writes are done with F(16))
0 = data read from selected module by controller (most data transfer reads are done with F(0))

(3) - 1 = control/test command to selected module (options bits F1-F4 completes command)
0 = data transfer command to selected module

Fig. 4 — NAF definition




Bit 0 = Dataway F1
Bit 1 = Dataway F2
Bit 2 = Dataway F4

During a data transfer Dataway Cycle (F8 = 0), these bits are gated onto the corresponding Dataway F lines.

Bit 3 = Inhibit Flip Flop. (Used to drive the Dataway I line).
Bit 4 = Inhibit. (Monitors the Dataway I line).

If bit 3 = 1, then 4 = 1, however, if bit 3 = 0, an external source of I may hold bit 4 = 1.

Bit 5 = X Interrupt Enable.

If bit 5 and bit 8 are set, any Dataway cycle in which X = 0 will cause an interrupt.

Bit 8 = Interrupt Enable.

If set, a LAM will cause an interrupt. In addition, if bit 5 = 1, a Dataway cycle where X = 0 will also cause an interrupt.

Bit 9 = LAM present. Signifies that one or more of the L lines is asserted.
Bit 11 = No read.

If set, the controller replies immediately to a DATI bus cycle to the Dataway and does generate a Dataway cycle. This bit must be set in order to execute a nondata transfer Dataway cycle.

All bits, except bit 4 and bit 9, can be overwritten. Bits 0, 3, 5, 8 and 11 are exclusively under control of the LSI-11. Bits 4, 6, 7 and 9 are additionally controlled by external events.

On B INIT, all bits are cleared except Inhibit Flip Flop (Bit 3) which is set.

Fig. 5 — Control/status register

The characteristics of Interleave Mode are:

a. User sends only one address to establish a link.
b. Performs read and write cycle under handler control.
c. Data is sent or received one item at a time.
d. Does not return to user until after the last read/write cycle.

When in the buffered mode, the user builds an IOTL consisting of any number of IOTB's. Each IOTB has a data buffer associated with it where up to 256 words of data my be written or retrieved.

## V HHTT Description

For the system upgrade, a device was required for remote monitoring and control without the need for bulky, expensive terminals or teletypewriters. This condition was satisfied by a portable pocket terminal which was designated the Hand Held Test Terminal (HHTT). The HHTT is used to command hardware devices in the local mode. The device is truly portable and may be connected to the RS232C port of any CAMAC crate. In addition to being a maintenance device, the HHTT is a "smart" device that can control operations in a CAMAC crate.

The HHTT chosen for our application is shown in figure 6. It is all solid-state, operates with RS232C or 20mA loop interfaces and is connected to the CAMAC system LSI 11/23 microprocessor through an Asynchronous Serial Port (ASP) interface module. This ASP interface consists of:

1) Crystal Clock

2) MIK-Bus Interface Circuits

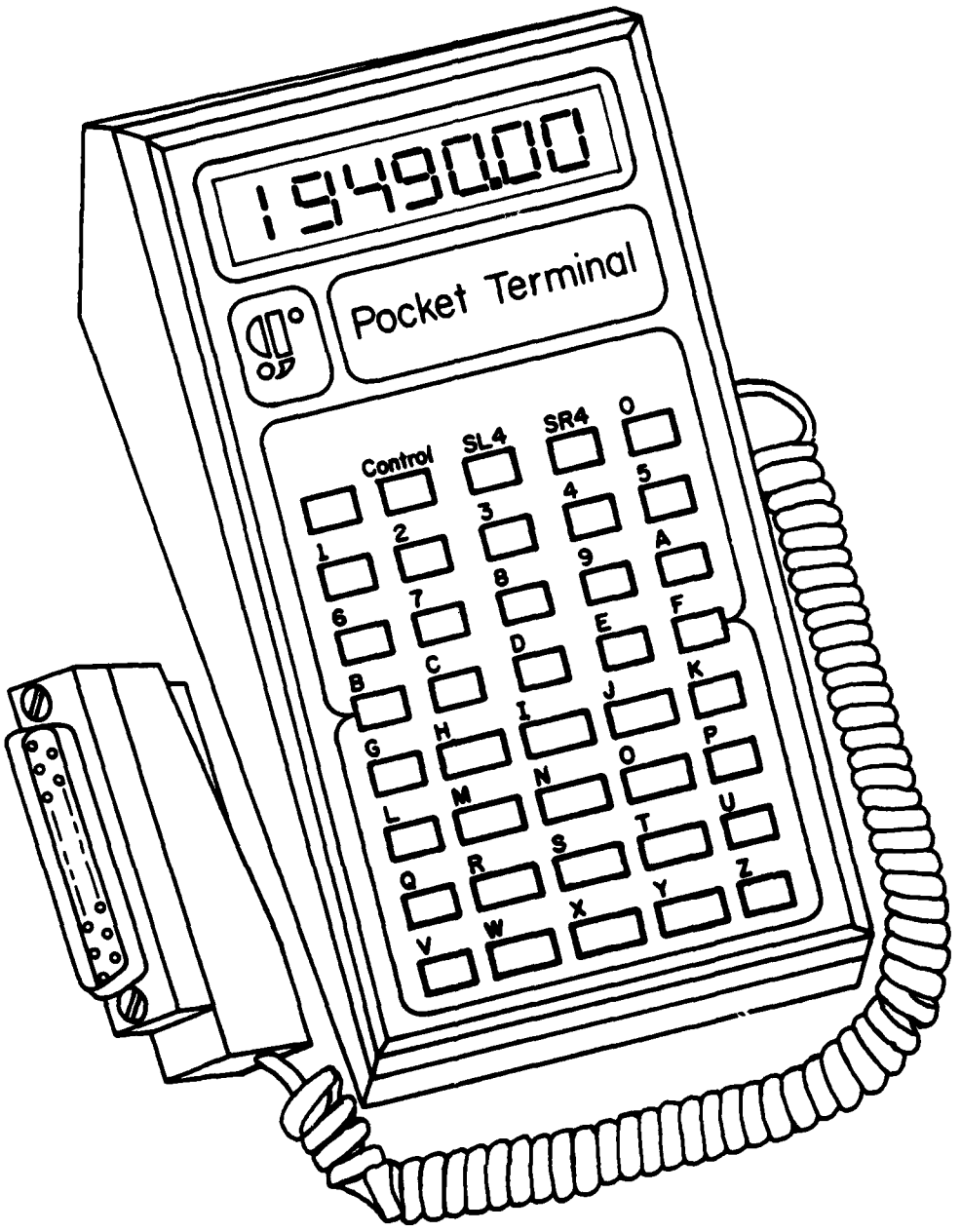



Fig. 6 — Hand Held Test Terminal (HHTT)

3) MOS/LSI asynchronous receiver/transmitter (UART) chip

4) EIA and 20mA DC loop level converters

The HHTT is a hand-held device capable of sending and receiving data in eight bit serial ASCII code. It has a 40-key positive tactile response keyboard. The keyboard provides two single function and 38 multi-function keys which give internal control of the unit and allow transmission of all 128 ASCII codes.

It incorporates a memory with capacity for the last 30 characters received. A line of eight consecutive characters in the memory can be accessed for simultaneous display on 16-segment-starburst LEDs. This starburst scheme can generate all 64 ASCII upper case alphanumerics and symbols. The ASCII codes generated by the HHTT are shown in figure 7. The ones that may be displayed are shown in figure 8 in their true appearance.

Two modes of display may be selected. In the first, data retrieved from the memory for display is entered at the right hand end of the memory line, 'shuffling' existing data one step left as each further character is received. Data may be entered in the second mode from the left hand end of the memory line a position controlled through formatting codes received from the host system. This allows data to be entered in any required format as well as permitting data already in the memory to be edited.

| bit 4 | bit 3 | bit 2 | bit 1 | bit 7 / bit 6 / bit 5 | 0 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1 0 0 | 1 0 1 | 1 1 0 | 1 1 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 0 | 0 | 0 | NUL | DLE | SP | 0 | @ | P | ` | p |
| 0 | 0 | 0 | 1 | 1 | SOH | DC1 | ! | 1 | A | Q | a | q |
| 0 | 0 | 1 | 0 | 2 | STX | DC2 | " | 2 | B | R | b | r |
| 0 | 0 | 1 | 1 | 3 | ETX | DC3 | # | 3 | C | S | c | s |
| 0 | 1 | 0 | 0 | 4 | EOT | DC4 | $ | 4 | D | T | d | t |
| 0 | 1 | 0 | 1 | 5 | ENQ | NAK | % | 5 | E | U | e | u |
| 0 | 1 | 1 | 0 | 6 | ACK | SYN | & | 6 | F | V | f | v |
| 0 | 1 | 1 | 1 | 7 | BEL | ETB | ' | 7 | G | W | g | w |
| 1 | 0 | 0 | 0 | 8 | BS | CU> | ( | 8 | H | X | h | x |
| 1 | 0 | 0 | 1 | 9 | HT | <CU | ) | 9 | I | Y | i | y |
| 1 | 0 | 1 | 0 | A | LF | SUB | * | : | J | Z | j | z |
| 1 | 0 | 1 | 1 | B | VT | ESC | + | , | K | [ | k | { |
| 1 | 1 | 0 | 0 | C | FF | FS | . | < | L | \ | l | ; |
| 1 | 1 | 0 | 1 | D | CR | GS | - | = | M | ] | m | } |
| 1 | 1 | 1 | 0 | E | SO | RS | . | > | N | ^ | n | ~ |
| 1 | 1 | 1 | 1 | F | SI | CLR | / | ? | O | ← | o | DEL |

Codes not displayed by Pocket Terminal are shown shaded.
NOTE: Bits sent in order shown in top, left hand section of table.

LEGEND

NUL null
SOH start of heading
STX start of text
ETX end of text
EOT end of transmission
ENQ enquiry
ACK acknowledge
BEL bell (audible signal)
BS back space
HT horizontal tab
LF line feed
VT vertical tab
FF form feed
CR carriage return
SO shift out
SI shift in
DLE data link escape
DC1 device control 1
DC2 device control 2
DC3 device control 3
DC4 device control 4
NAK negative acknowledge
SYN synchronous idle
ETB end of transmission block
CU> cursor right step
<CU cursor left step
SUB substitute
ESC escape
FS file separator
GS group separator
RS record separator
CLR display clear
SP space
DEL rub out

**Fig. 7 — ASCII codes generated by pocket terminal**

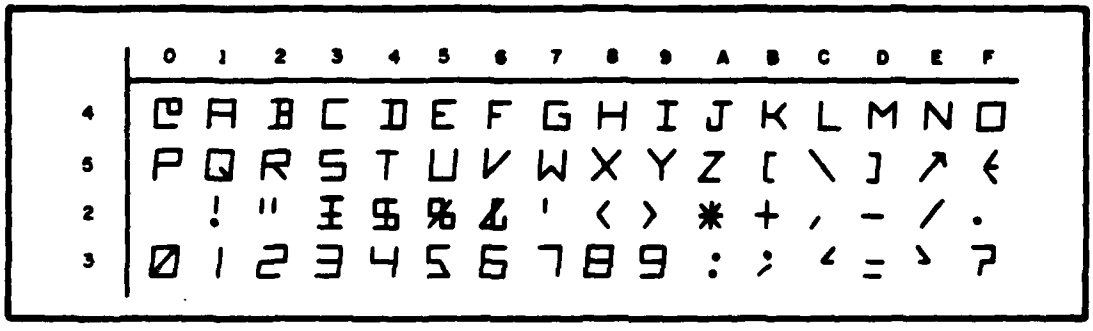



Fig. 8 — ASCII set generated by 16-segment LEDs

## VI The HHTT Users Guide

The purpose of this section is to provide instructions for the use of the HHTT in performing Control/Transfer Commands (CTCs) and Data Transfer Commands (DTCs). The HHTT is used to command hardware devices on the CAMAC Dataway in the local mode. Command arguments will be entered in decimal.

The HHTT Service Routine, similar to other service routines, loads an IOTB and calls the I/O Handler to perform I/O on the CAMAC Dataway. Most of the IOTB is pre-loaded by the HHTT Service Routine. The rest is entered by the operator. The HHTT is limited to doing 16 bit word length I/O in the bufferd mode with one IOTB. If an error is made in the procedure at any time, the operator may enter @ and start over from the beginning. If the operator wants to discontinue the use of the HHTT at any time he may do so by entering an E (Exit).

The operator may cause an interrupt to the Controller Monitor by pressing "G" on the HHTT keyboard when the HHTT is connected to the CAMAC Chassis. The message "Press C" will be displayed and, at this time, CAMAC Chassis Controller diagnostics may be executed or a command and/or data transfer may be initiated. If a one (1) is entered, the LSI 11/23 memory, LSI 11/23 instruction set, and CPU interface card will be tested for errors, and the CAMAC Chassis Controller status word will be displayed. To initiate a command or a data transfer, first a C is entered when the message "Press C" is displayed. If "C" is not entered, a message "W-RETRY" meaning "WRONG CHARACTER - TRY AGAIN" is displayed. The operator is then prompted for the transfer count, station number, subaddress, and function code. These are all entered in decimal values. If a character other than 0-9 is entered for those values, an illegal character message "I - RETRY" meaning ILLEGAL CHARACTER - RETRY is displayed.

At this point the IOTB is configured with the necessary information to call the I/O Handler to perform the transfer. The following table explains these prompts:

| PROMPT | MEANING |
|---|---|
| 1. T(00-99 | Word Transfer count (DTC = 01 to 99, CTC=00) |
| 2. N(01-25 | Station Number (Range of 01 to 25) |
| 3. A(00-15 | Subaddress (Range of 00 to 15) |
| 4. F(00-31 | Function Code (Range of 00 to 31) |

If a CTC is requested it will be performed, the HHTT will exit to the Controller and the operator must enter a G to input another command. If an error occurs during the transfer, the bell will sound, a message "ERROR" will be displayed for approximately 3 seconds, and the message "PRESS C" is displayed. The command may then be retried. The transfer count should be ØØ for a CTC. After the CTC is performed, the HHTT routine exits to the Controller Monitor and a G must be entered to initiate another command.

If a DTC is requested, the message "PRESS D" will be displayed and the next character entered must be a D to initiate the DTC. If the next character is not a D the message " W-RETRY" for WRONG CHARACTER - TRY AGAIN will be displayed until the operator enters a D.

If a write operation is required the message "O, D, or H?" will be displayed and the operator must choose the number system of the data to be entered. An entry of O means that the data will be octal (base eight), an entry of D means that the data will be decimal (base ten), and an entry of H means that the data will be hexadecimal (base sixteen).

After the number system is chosen, the message "DATA?" will be displayed and the operator must enter data one item at a time with a comma (,) between each data item. A carriage return (CR) terminates the transfers. The maximum single octal value that may be entered is 177777, the maximum single decimal value that may be entered is 65535, and the maximum single hexadecimal value that may be entered is FFFF. The limiting factor for these values is the 16 bit word size of the LSI 11/23. The user is responsible for seeing that overflow does not occur.

Once the number system is chosen, the only legal octal digits are 0 - 7, the only legal decimal digits are 0 - 9, and the only legal hexadecimal digits are 0 - 9 and A - F. If a character other than a legal digit is entered, a message "I-RETRY" for ILLEGAL CHARACTER - RETRY is displayed. The HHTT software always operates in the buffered mode and will transfer the number of items entered for the transfer count. After the end-of-data character (CR) is pressed, the complete buffer of stored values are written to the target module. If an error occurs during the write, the bell will sound, the message "ERROR" will be displayed for approximately 3 seconds, the message "ENTER C" is displayed, and the command may be retried. After the write operation is performed, the HHTT routine exists to the Controller Monitor and a G must be entered to initiate another command.

If a read operation is requested, it will be performed after the D is entered and the data will come to the HHTT Service Routine Data Buffer. The message "O, D, or H?" will be displayed and the operator must choose the number system for the display of the data. An entry of O means that the data will be displayed in octal, an entry of D means that the data will be displayed in decimal, and an entry of H means that the data will be displayed in hexadecimal. After the

number system is chosen, the HHTT data buffer is converted to ASCII and moved to an ASCII buffer where it can be displayed by the operator. A message "PRESS M" is displayed and the operator must press M to display the first word of data followed by a comma (,). Each successive word may then be displayed one at a time followed by a comma (,) as M is pressed for each word. After all data items are displayed, the message "DONE" will be displayed. If an error occurs during the read operation, the bell will sound, the message "ERROR" will be displayed for approximately 3 seconds, and the message "ENTER C" is displayed. The command may then be retried. After the read is performed, the HHTT routine exists to the Controller Monitor and a G must be entered to initiate another command.

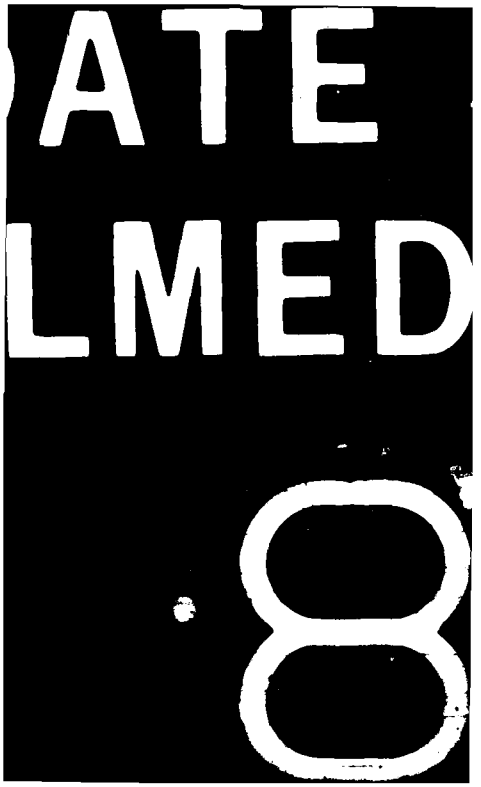
## VII Summary

This design has been implemented at test facilities and is scheduled to be deployed at world-wide sites in early 1983. Initial analysis indicates the major objective - to improve software/hardware maintainability, capabilities, and operability - is being achieved.

The modular system feature provided by CAMAC has permitted the use of the latest microelectronics technology in the system upgrade. Modules are being constructed with integrated circuit packages of high component-packing density. This has made it possible to build compact and efficient modules which may be removed and replaced without removing adjacent modules.

One of the requirements levied during the initial design phase was that all dataway communications between modules would be through the CAMAC controller. The CAMAC I/O Handler is being used to satisfactorily fulfill this requirement.

Another requirement levied during the initial design phase was that a standard RS232 interface link would be provided for each CAMAC crate. This link would allow the transfer of data and controls for a local mode of operation. The HHTT and it's accompanying software has provided a very adequate solution to this problem.


ATE
LMED
8